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Integral form 4-D light field filters using Xilinx FPGAs and 45 nm CMOS technology

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Abstract Four-dimensional (4-D) infinite impulse response frequency hyper-planar filter and a digital VLSI architecture for real time light field based depth filtering applications is proposed. A signal flow graph based on discrete spatial integrators is introduced, which leads to improved sensitivity properties for perturbations in filter coefficients. First order sensitivity analysis of filter transfer function shows a 92.9 % reduction of maximum gain error in frequency response with 12 bits of fractional precision, when compared with a direct-form architecture. Prototype FPGA hardware-in-the-loop co-simulations are performed for two different light field geometries. Register transfer level design validation is carried out via FPGA hardware emulation with a host computer providing memory buffers, and the full-design emulation is carried out on a standalone Berkely Emulation Engine (BEE3), operating at 36.44 and 37.31 MHz for the two light field geometries, respectively. 45 nm CMOS implementation is carried out up to the synthesis level, yielding operating frequencies of 154.4 and 153.3 MHz (correspondingly frame rates of 1.15 and 18.286 Hz) for the two light field geometries, respectively.

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1 Introduction

The continued scaling of deep sub-micron digital CMOS technology and the accompanying increase in density for both application specific integrated circuits (ASICs) and field-programmable gate arrays (FPGAs) have lead to new possibilities for VLSI digital filters. A particular area of growth is the real-time digital and mixed-signal implementation of high-performance multi-dimensional (MD) digital filters (Arjuna Madanayake et al. 2008). We explore the potential use of four-dimensional (4-D) infinite impulse response (IIR) digital filters in light field based depth filtering, with possible applications in intelligent video surveillance, traffic monitoring, machine vision, industrial automation, and robotics. In this work, we propose a low-sensitivity integral-form signal flow graph (SFG) (Proakis 2001) and digital VLSI architecture for 4-D IIR light field digital filters.

Light fields are a MD representation of the light permeating a scene, allowing efficient synthesis of rendered views (Levoy and Hanrahan 1996) and has lead to new applications in machine vision. Emerging algorithms exploit light fields to accomplish complex tasks such as depth filtering, distractor isolation, visual odometry and tracking through occlusions (Dansereau and Bruton 2003; Dansereau et al. 2011; Dansereau and Williams 2011; Joshi et al. 2007). A light field is recorded by constructing a planar array of cameras (Wilburn et al. 2004, 2005), as depicted in Fig. 1, by moving a camera to each grid-point $(n_1, n_2) \in \mathbb{N}^2$ (Wilburn et al. 2002), or through the use of lenticular arrays or modulating masks (Ng et al. 2005; Veeraraghavan et al. 2007).

Recently, the use of differential operators in light field filtering has been shown to lead to low complexity hardware compared to direct-form filters (Madanayake et al. 2012). In this scheme, spatial delays are replaced by 1-D differentiators operating on each of the four light field dimensions. To the best of our knowledge, apart from Madanayake et al. (2011), Madanayake (2008), Madanayake et al. (2012) and Wimalagunaratne et al. (2012), no other 4-D IIR digital filters have been previously reported. The goal of the present work is to study the use of *integral* operators in 4-D IIR filter hardware with the specific desire of reducing the sensitivity of the 4-D filter transfer functions to perturbations in the filter coefficients. Such perturbations arise from quantization of filter coefficients in fixed-point digital arithmetic realizations, and can seriously impede filter operation.

Light fields parametrize light within a scene in terms of four dimensions. As shown in Fig. 1, these dimensions correspond to camera position $(n_1, n_2) \in \mathbb{N}^2$, and pixel location for a camera $(n_3, n_4) \in \mathbb{N}^2$ leading to the light field function $L(\mathbf{n})$, where $\mathbf{n} \equiv (n_1, n_2, n_3, n_4) \in \mathbb{N}^4$. To date, most reported light field processing has been demonstrated in software. The large data volumes and high parallelism of light field processing makes it an excellent candidate for digital hardware VLSI implementation having the advantages of increased speed, lower power consumption and smaller form factors, enabling deployment in embedded applications. A natural candidate for hardware implementation is a class of 4-D filters designed for depth filtering. In Dansereau and Bruton (2003), it was shown that a light field can be selectively filtered for a specific depth by using a 4-D IIR filter having a frequency-hyperplanar passband with appropriately selected orientation. In this work, we propose a practical-BIBO stable (Agathoklis and Bruton 1983; Xu et al. 2003; Lin and Bruton 1989) low-sensitivity digital hardware realization for such 4-D IIR *frequency-hyperplanar digital filters*, based on discrete domain spatial integral operators. An overview of the proposed system is shown in Fig. 1, in which two frequency-hyperplanar digital filters having the 4-D $\mathbf{z}$-domain transfer functions

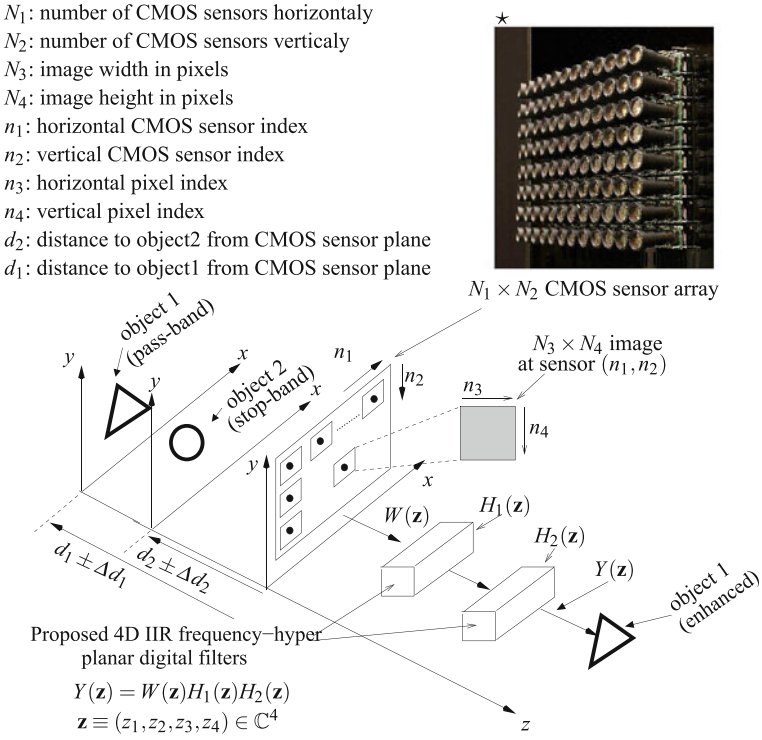

Fig. 1 Overview of light field based depth filtering using 4-D IIR frequency-hyperplanar filters (Dansereau and Bruton 2007) (⋆ photo from Stanford University)

$H_1(\mathbf{z})$ and $H_2(\mathbf{z})$ are used to perform the depth filtering. Here $\mathbf{z} \equiv (z_1, z_2, z_3, z_4) \in \mathbb{C}^4$ defines the 4-D $\mathbf{z}$-transform domain where $z_q = e^{s_q} \in \mathbb{C}, s_q = \sigma_q + j\omega_q \in \mathbb{C}$ with ω_q being the frequency variable along the dimension n_q, where $q \in \{1, 2, 3, 4\}$. For certain depth filtering applications, the two filters $H_1(\mathbf{z})$ and $H_2(\mathbf{z})$ can both be reduced to 2-D filters (Dansereau and Bruton 2007). In this paper, we consider the general case, where both $H_1(\mathbf{z})$ and $H_2(\mathbf{z})$ are 4-D filters. We provide a low-sensitivity *integral-form* SFG based on discrete spatial integrators (Strecker and Bruton 1983), as well as an FPGA and custom silicon implementation up to the synthesis level at the 45 nm CMOS technology. The proposed hardware architecture is implemented as a single centralized processing unit, that processes the 4-D light field input data in a raster scanned fashion. To wit, we exploit the well-known property of relatively low sensitivity to coefficient quantization of integral form filters in this 4-D IIR filter design problem. We make use of 1st-order multi-parameter sensitivity theory (Bruton 1980, ISBN:0-13-753467-1) to show that our proposed SFG has lower sensitivity to finite precision quantization effects in the filter coefficients than direct-form SFGs.

The rest of this paper is organized as follows. Section 2 is a review of light fields and 4-D IIR frequency-planar filters. Section 3 describes the proposed filter architecture and compares with direct-form SFGs in terms of transfer function sensitivity. In Sect. 4 we present the prototype implementation on a Xilinx Virtex-6 FPGA device. We present experimental verification of the implementation in Sect. 5, on both a host-embedded FPGA and a standalone Berkeley Emulation Engine (BEE3). Finally, Sect. 6 concludes the paper.

2 Light fields and 4-D frequency-hyperplanar filters

Light fields exhibit a set of convenient characteristics which make linear depth filtering possible. In particular, a scene containing Lambertian surfaces at a single depth will exist as a set of parallel planes in the light field, with the orientations of the planes depending on the depth of the surfaces in the scene (Dansereau and Bruton 2003). It is recalled that, a perfectly matte surface is often referred to as a Lambertian surface because, based on the Lambert's cosine law, it can be shown that the luminance of emanating light from such a surface is independent from the viewing angle (Dansereau 2003). By superposition, a scene containing surfaces at multiple depths will exist as planes at multiple orientations, therefore, filtering for a specific plane orientation is equivalent to filtering for a specific depth.

Another convenient light field characteristic is that parallel planes in the light field have a frequency-domain region of support (ROS) which is a plane passing through the frequency origin. Here $\boldsymbol{\omega} \equiv (\omega_1, \omega_2, \omega_3, \omega_4) \in \mathbb{R}^4$ denotes the 4-D frequency domain, where $\omega_q, q = 1, 2, 3, 4$ correspond to the frequency variable along the dimensions n_1, n_2, n_3, n_4, respectively. The orientation of the frequency-domain ROS depends on the orientation of the spatial-domain planes, and therefore on the depth of the scene's surfaces. Filtering for a specific depth in a scene, then, can be accomplished by filtering for a specific plane orientation in $\boldsymbol{\omega}$. This is most simply accomplished by cascading appropriately-oriented frequency- *hyperplanar* filters $H_1(\mathbf{z})$ and $H_2(\mathbf{z})$, as shown in Fig. 1. Both $H_1(\mathbf{z})$ and $H_2(\mathbf{z})$ have frequency-hyperplanar passbands given by $P_1 \equiv \mathbf{L_1^T}\omega = 0$ and $P_2 \equiv \mathbf{L_2^T}\omega = 0$, respectively in $\boldsymbol{\omega}$. By cascading $H_1(\mathbf{z})$ and $H_2(\mathbf{z})$ a frequency-planar passband in $\boldsymbol{\omega}$ given by $P_1 \cdot P_2 = (\mathbf{L_1^T}\omega) \cdot (\mathbf{L_2^T}\omega) = 0$ is formed which can effectively encompass spectrum of the light field corresponding to the desired depth. The orientation of the resulting frequency-planar passband $P_1 \cdot P_2$ is controlled by selecting $\mathbf{L_i} = [L_{i1} L_{i2} L_{i3} L_{i4}]^\top, i = 1, 2$, appropriately.

We will next present the transfer function and implementation details of the frequency-hyperplanar filter $H_1(\mathbf{z})$ for a given passband orientation specified by $\mathbf{L_1}$. Design and implementation of $H_2(\mathbf{z})$ follows the same approach, with the passband orientation specified by $\mathbf{L_2}$. Both $\mathbf{L_1}$ and $\mathbf{L_2}$ can be evaluated based on the light field parameters of the particular depth filtering application as described in Dansereau (2003).

2.1 Frequency-hyperplanar filter

A continuous-domain 1st-order frequency-hyperplanar filter can be represented using a 4-D inductance resistance network with a resistive termination (Bruton and Bartley 1985). The 4-D Laplace transform of the input output transfer function of this filter is given as

$$H_1(\mathbf{s}) = \frac{R_0}{R_0 + L_{11}s_1 + L_{12}s_2 + L_{13}s_3 + L_{14}s_4} \equiv \frac{Y(\mathbf{s})}{X(\mathbf{s})}, \tag{1}$$

where $\boldsymbol{s} \equiv (s_1, s_2, s_3, s_4) \in \mathbb{C}^4$ denotes the 4-D Laplace domain, $R_0 > 0$ and $L_{1q} > 0$, $q = 1, 2, 3, 4$ (Bruton and Bartley 1985). $H_1(\mathbf{s})$ exhibits resonance along a 4-D hyperplane passing through the origin in $\boldsymbol{\omega}$ (Dansereau and Bruton 2003) given by

$$\omega_1 L_{11} + \omega_2 L_{12} + \omega_3 L_{13} + \omega_4 L_{14} = 0. \tag{2}$$

By appropriately selecting the passive components $L_{1q}, q = 1, 2, 3, 4$ in (1), and cascading two transfer functions, we obtain the overall passband described by the product $H_1(\mathbf{s}) \cdot H_2(\mathbf{s})$. This passband selectively passes spectral components corresponding to

scene elements at the desired depth, while attenuating spectral components corresponding to elements outside the desired depth (Dansereau 2003).

By applying the normalized 4-D bilinear transform (BLT), $s_q = \left(1 - z_q^{-1}\right)/\left(1 + z_q^{-1}\right)$, $q = 1, 2, 3, 4$, we obtain the *direct-form* 4-D IIR frequency-hyperplanar **z**-domain transfer function

$$H_1(\mathbf{z}) = \frac{\prod_{q=1}^{4}\left(1 + z_q^{-1}\right)}{1 + \underbrace{\sum_{k=0}^{1}\sum_{l=0}^{1}\sum_{m=0}^{1}\sum_{n=0}^{1} d_{klmn} z_1^{-k} z_2^{-l} z_3^{-m} z_4^{-n}}_{k+l+m+n\neq 0}}, \tag{3}$$

where the direct-form filter coefficients d_{klmn} are given by

$$d_{klmn} \equiv \frac{\left(R + (-1)^k L_{11} + (-1)^l L_{12} + (-1)^m L_{13} + (-1)^n L_{14}\right)}{(R + L_{11} + L_{12} + L_{13} + L_{14})}. \tag{4}$$

We replace discrete domain delay operators having the **z**-transform z_q^{-1}, $q = 1, 2, 3, 4$ in (3) with discrete spatial integral operators w_q^{-1} given by Reddy et al. (1996), Khoo et al. (2006), Khoo and Reddy (2008)

$$w_q^{-1} = \frac{z_q^{-1}}{1 - z_q^{-1}}, \quad q = 1, 2, 3, 4$$

to obtain the proposed transfer function

$$H_1(\mathbf{z}) = \frac{\sum_{k=0}^{1}\sum_{l=0}^{1}\sum_{m=0}^{1}\sum_{n=0}^{1} a_{klmn} w_1^{-k} w_2^{-l} w_3^{-m} w_4^{-n}}{1 + \underbrace{\sum_{k=0}^{1}\sum_{l=0}^{1}\sum_{m=0}^{1}\sum_{n=0}^{1} b_{klmn} w_1^{-k} w_2^{-l} w_3^{-m} w_4^{-n}}_{k+l+m+n\neq 0}}. \tag{5}$$

The integral-form filter coefficients a_{klmn} and b_{klmn} are found by equating (3) and (5) and comparing the numerators and denominators (Strecker and Bruton 1983). From the numerators we obtain

$$a_{klmn} = \begin{cases} 1 & k+l+m+n = 0 \\ 2 & k+l+m+n = 1 \\ 4 & k+l+m+n = 2 \\ 8 & k+l+m+n = 3 \\ 16 & k+l+m+n = 4 \end{cases}, \tag{6}$$

where $k \in \{0, 1\}, l \in \{0, 1\}, m \in \{0, 1\}, n \in \{0, 1\}$. From the denominators we obtain

$$\begin{aligned} b_{klmn} = \lambda\{ & R + (-1)^k L_{11} + (-1)^l L_{12} + (-1)^m L_{13} + (-1)^n L_{14} \\ & + (-1)^{k+l+m+n}\alpha\left[lb_{0100} + kb_{1000} + mb_{0010} + nb_{0001}\right] \\ & - (-1)^{k+l+m+n}\beta\left[kmb_{1010} + mnb_{0011} + knb_{1001} + klb_{1100} + lnb_{0101} + lmb_{0110}\right] \\ & + (-1)^{k+l+m+n}\mu\left[kmnb_{1011} + lmnb_{0111} + klnb_{1101} + klmb_{1110}\right]\} \end{aligned} \tag{7}$$

$$\alpha = \begin{cases} 1 & k+l+m+n > 1 \\ 0 & else \end{cases}, \tag{8}$$

$$\beta = \begin{cases} 1 & k+l+m+n > 2 \\ 0 & else \end{cases}, \tag{9}$$

$$\mu = \begin{cases} 1 & k+l+m+n > 3 \\ 0 & else \end{cases}, \tag{10}$$

where $\lambda = 1/b_{0000}$.

3 Raster-scanned 4-D filter architecture

3.1 Integral-form signal flow graph

As shown in Fig. 1, the input light field to $H_1(\mathbf{z})$ is a $(N_1 \times N_2 \times N_3 \times N_4)$ 4-D hypercube of data points denoted by $w(\mathbf{n})$. For the proposed raster scan filter architecture, we obtain an input stream $w_{SCAN}(\tau)$ by raster scanning the 4-D data volume $w(\mathbf{n})$ with the index mapping $\tau = N_1N_2N_3n_4 + N_1N_2n_3 + N_1n_2 + n_1$. The filtered output stream of data is denoted by $y_{SCAN}(\tau)$. The operating frequency of the filter is $F_{CLK} = \Delta T_S/N_1N_2N_3$, where ΔT_S is the uniform volume-frame sample time.

The proposed SFG is shown in Fig. 2a, where the required zero initial condition (ZIC) blocks are denoted in Fig. 2b. These ZIC blocks are implemented by combining spatial-delay processors (SDPs) with spatial integrator blocks (Madanayake and Bruton 2006), where an SDP presents a zero value when required, and pass the input signal unchanged otherwise (Madanayake and Bruton 2006; Madanayake 2008). The architecture requires 30 parallel multipliers, 45 two-input adders, 1 volume-array clocked first-in-first-out (FIFO) buffer Γ of length $N_1N_2N_3$—representing the major part of the memory resources—two SDP_D, four SDP_C, and eight SDP_R circuits, which are used to provide the ZICs required by p-BIBO stability (Agathoklis and Bruton 1983; Xu et al. 2003; Lin and Bruton 1989) of the filter. Column- and row-wise ZICs are achieved using column and row SDP circuits, denoted by SDP_C and SDP_R, respectively (Madanayake and Bruton 2006). A depth-wise spatial delay processor SDP_D, that is a 4-D extension of SDPs in Madanayake and Bruton (2006) is depicted in Fig. 2.

The details of the SDP circuits shown in Fig. 2b are described in Fig. 3. The column-wise SDPs (SDP_C) force the output of the SDP circuit to be zero whenever $n_1 = 0$, otherwise the input is passed forward. As shown in Fig. 3a, when the counter value becomes zero, it implies that $n_1 = 0$. Row-wise SDPs (SDP_R) force the output of the SDP circuit to be zero whenever $n_2 = 0$, otherwise the input is passed forward. As shown in Fig. 3b, when the counter value becomes less than N_1, zeros are sent out of the multiplexer circuit and it implies that $n_2 = 0$. Depth-wise SDPs (SDP_D) shown in Fig. 3c force the output of the SDP circuit to be zero whenever $n_3 = 0$, otherwise the input is passed forward.

3.2 Transfer function sensitivity analysis

The 1st-order sensitivity of $H_1(\boldsymbol{\omega})$ for filter coefficients γ is defined in Bruton (1980, ISBN: 0-13-753467-1) as

$$S_{\gamma}^{H_1(\boldsymbol{\omega})} = \frac{\gamma}{H_1(\boldsymbol{\omega})} \frac{\partial H_1(\boldsymbol{\omega})}{\partial \gamma}. \tag{11}$$

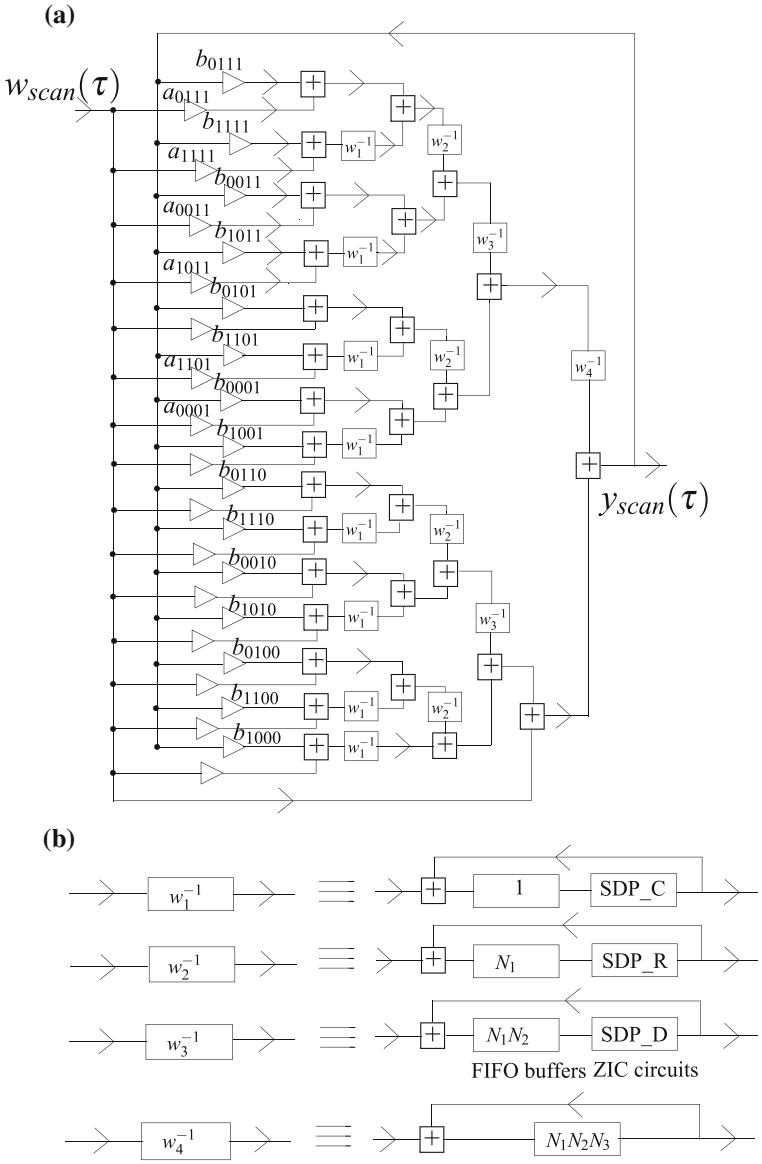

Fig. 2 **a** Proposed integral-form SFG ($\tau = (n_4)N_1N_2N_3 + (n_3)N_1N_2 + (n_2)N_1 + n1$); **b** block definitions used in the SFG

Letting $G(\boldsymbol{\omega}) = |H_1(\boldsymbol{\omega})|$, the gain sensitivity with respect to coefficient γ is defined as, $S_\gamma^{G(\boldsymbol{\omega})} = Re\left[S_\gamma^{H_1(\boldsymbol{\omega})}\right]$ (Bruton 1980, ISBN:0-13-753467-1), and the percentage gain error due to $\Delta\gamma$ perturbations in coefficient γ is given by

$$\frac{\Delta G(\boldsymbol{\omega})}{G(\boldsymbol{\omega})} = S_\gamma^{G(\boldsymbol{\omega})}\left(\frac{\Delta\gamma}{\gamma}\right) \times 100\,\%. \tag{12}$$

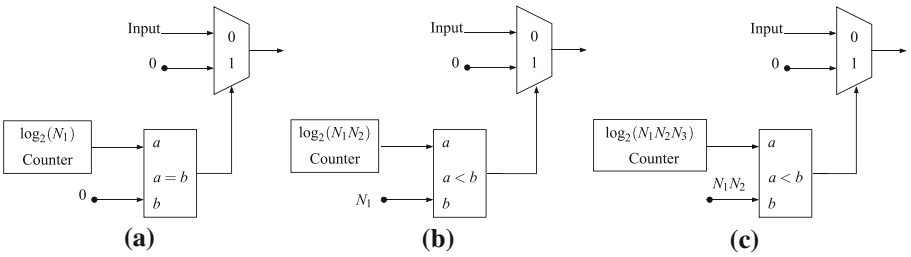

Fig. 3 Required spatial delay processors: **a** SDP_C, **b** SDP_R, and **c** SDP_D

3.2.1 Direct form sensitivity

Following (3) and (11), we obtain the gain sensitivity of direct-form $H_1(\mathbf{z})$ in (3) with respect to numerator coefficients a_{klmn} and denominator coefficients d_{klmn} as given by:

$$S^{G(\omega)}_{a_{klmn}}(\boldsymbol{\omega}) \approx Re\left\{\frac{e^{-j(k\omega_1+l\omega_2+m\omega_3+n\omega_4)}}{N(\boldsymbol{\omega})}\right\} a_{klmn}, \tag{13}$$

$$S^{G(\omega)}_{d_{klmn}}(\boldsymbol{\omega}) \approx Re\left\{-\frac{e^{-j(k\omega_1+l\omega_2+m\omega_3+n\omega_4)}}{D(\boldsymbol{\omega})}\right\} d_{klmn}, \tag{14}$$

where $N(\boldsymbol{\omega})$ and $D(\boldsymbol{\omega})$ are the numerator and denominator polynomials of the direct-form transfer function $H_1(\mathbf{z})$ in (3) evaluated on the unit 4-D hypercircle $z_q = e^{j\omega_q}$, $q = 1, 2, 3, 4$. Note that for direct-form, the numerator coefficients $a_{klmn} = 1\,\forall\, k, l, m, n$.

3.2.2 Integral form sensitivity

Similar expressions for the gain sensitivity of the integral-form $H_1(\mathbf{z})$ given in (5) with respect to numerator and denominator coefficients are given by (15) and (16), respectively, where $P(\boldsymbol{\omega})$ and $Q(\boldsymbol{\omega})$ are the numerator and denominator polynomials of the integral-form transfer function $H_1(\mathbf{z})$ in (5), evaluated on the unit 4-D hypercircle $z_q = e^{j\omega_q}$, $q = 1, 2, 3, 4$

$$S^{G(\omega)}_{a_{klmn}}(\boldsymbol{\omega}) \approx Re\left\{-\frac{(e^{j\omega_1}-1)^{-k}(e^{j\omega_2}-1)^{-l}(e^{j\omega_3}-1)^{-m}(e^{j\omega_4}-1)^{-n}}{P(\boldsymbol{\omega})}\right\} a_{klmn} \tag{15}$$

$$S^{G(\omega)}_{b_{klmn}}(\boldsymbol{\omega}) \approx Re\left\{-\frac{(e^{j\omega_1}-1)^{-k}(e^{j\omega_2}-1)^{-l}(e^{j\omega_3}-1)^{-m}(e^{j\omega_4}-1)^{-n}}{Q(\boldsymbol{\omega})}\right\} b_{klmn} \tag{16}$$

Figure 4 shows the maximum value of the gain sensitivity for direct-form and integral-form transfer functions with respect to their denominator coefficients given by (14) and (16), respectively. We observe for $klmn \in \{0011, 0101, 0110, 1001, 1010, 1011, 1100, 1101, 1110\}$ the integral form exhibits lower sensitivity, which we will now demonstrate leads to reduced maximum gain error.

3.3 Maximum percentage gain error

Let D_c be the fractional precision used to implement the filter coefficients in digital hardware. Rounding quantization error leads to a maximum error in filter coefficients

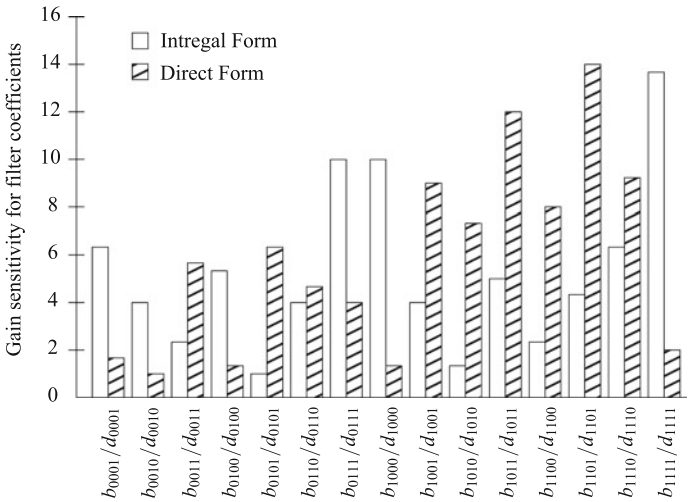

Fig. 4 Maximum value of the gain sensitivity of direct- and integral-form transfer functions to their denominator coefficients

$\Delta a_{klmn} = \Delta b_{klmn} = \Delta d_{klmn} = 2^{-(D_c+1)}$, and will be reflected as error in the magnitude frequency response $G(\boldsymbol{\omega})$. We define $E(\boldsymbol{\omega})$ given by (17) as the maximum percentage error in magnitude response and use $E(\boldsymbol{\omega})$ as a metric to compare the sensitivity properties of the direct-form and proposed integral-form transfer functions,

$$E(\boldsymbol{\omega}) = \sum_{(k,l,m,n)=0}^{1} \left[S_{a_{klmn}}^{G(\boldsymbol{\omega})} \frac{\Delta a_{klmn}}{a_{klmn}} + S_{b_{klmn}}^{G(\boldsymbol{\omega})} \frac{\Delta b_{klmn}}{b_{klmn}} \right] 100\,\%. \tag{17}$$

Figure 5 shows $E(\boldsymbol{\omega})$ for both direct- and integral-form transfer functions evaluated at different frequency slices for $D_c = 12$ bits. We observe that the integral form exhibits significantly lower gain error for the same fractional fixed-point precision. Furthermore, by computing the maximum value of $E(\boldsymbol{\omega})$ we obtain for integral form a maximum error $Max[E(\boldsymbol{\omega})] = 0.1602\,\%$ and for direct form $Max[E(\boldsymbol{\omega})] = 2.2866\,\%$, demonstrating a 92.9 % reduction in the maximum percentage gain error for $D_c = 12$ bits in the proposed integral-form SFG.

4 Prototype FPGA implementation

We implemented the proposed raster-scanned integral-form SFG shown in Fig. 2 on a Xilinx Virtex-6 xc6vlx240t-1ff1156 FPGA device installed on a Xilinx ML605 development board. In Table 1, we provide the FPGA implementation parameters used. By using a unit impulse input for $w_{SCAN}(\tau)$, we obtain the impulse response $h_1(\mathbf{n})$ of the proposed 4-D IIR integral-form frequency-hyperplanar filter by using the bit-true-cycle-accurate hardware-in-the-loop co-simulation (HCS) facility in Xilinx System Generator (XSG). We then compute the 4-D discrete Fourier transform (DFT) of $h_1(\mathbf{n})$ to obtain the frequency response shown in Fig. 6.

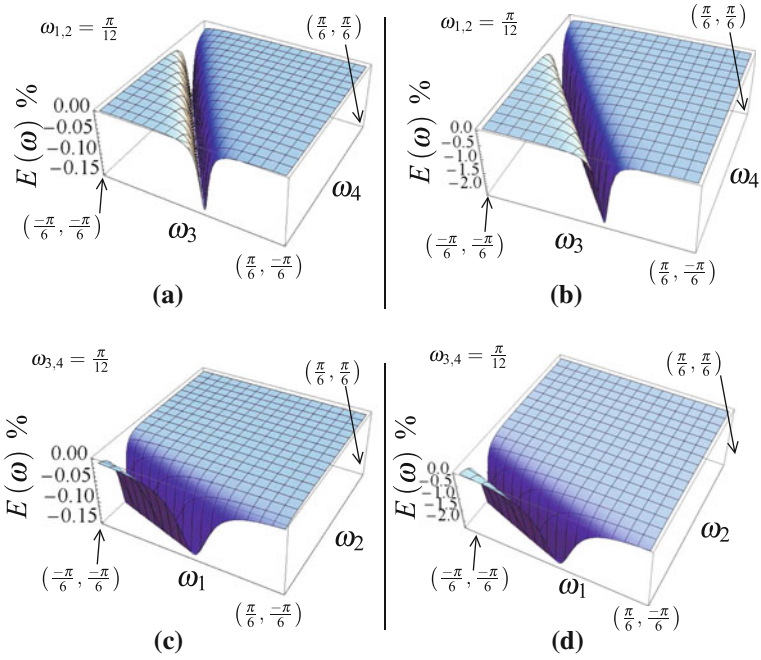

Fig. 5 Percentage gain error $E(\boldsymbol{\omega})$ in (17) evaluated at $\omega_{1,2} = \pi/12$ for **a** integral-form and **b** direct-form filters. $E(\boldsymbol{\omega})$ in (17) evaluated at $\omega_{3,4} = \pi/12$ for **c** integral-form (proposed) and **d** direct-form filters (Wimalagunaratne et al. 2012; Madanayake et al. 2011)

Table 1 FPGA resources and parameters for example 1 and example 2 designs in the Xilinx ML605 FPGA prototyping system

	Example 1		Example 2	
	$H_1(z)$	$H_2(z)$	$H_1(z)$	$H_2(z)$
Max frequency (MHz)	34.238	34.713	34.382	35.871
Number of slice LUTs	5,690	5,683	11,595	10,989
Number of slice registers	1,025	1,025	2,862	2,829
Number of occupied slices	1,461	1,466	3,141	2,911
Number of LUT flip flop pairs	5,690	5,683	11,595	10,989
Number of DSP48s	86	86	297	297

4.1 VLSI resource consumption and critical path delay

If the VLSI hardware requirements for W-bit multipliers and adders/subtracters are γ_M, and γ_A, respectively, then the total VLSI resource consumption of the proposed SFG in Fig. 2 is approximated by $\gamma_T \approx 30\gamma_M + 45\gamma_A + N_1N_2N_3K_0 + K_1$, where K_0 denotes the total VLSI resource requirements of a single-bit FIFO buffer, and K_1 denotes the VLSI resource requirements for the ZIC circuits shown in Fig. 2b.

The minimum critical path delay of the circuit, after employing pipelining, is given by $T_{CPD} \approx T_M + 2T_A + T_{MUX}$, where T_M, T_A and T_{MUX} are the propagation delays of a parallel multiplier, adder/subtractor, and two-input $W-$bit multiplexer, respectively. Therefore, the maximum clock frequency is $F_{CLK,Max} = 1/T_{CPD}$.

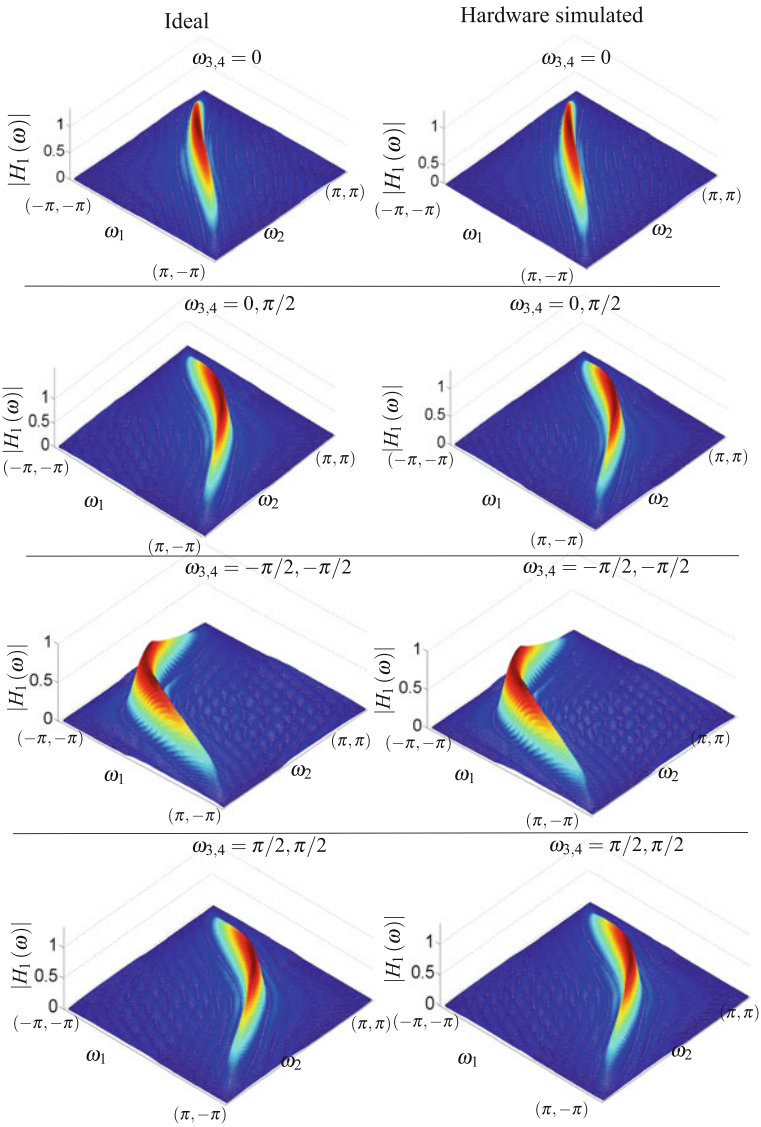

Fig. 6 Column one corresponds to a 2-D slice at various ω_3, ω_4 values of the ideal magnitude frequency response $|H_1(\boldsymbol{\omega})|$ obtained by computing the DFT of the unit impulse response $h_1(\mathbf{n})$. Similarly, column two corresponds to the magnitude frequency response calculated from the unit impulse output of the prototype FPGA implementation

4.2 Estimated real-time throughput

The real-time throughput is $30F_{CLK}$ fixed-point multiplications and additions/subtractions of $45F_{CLK}$ per second, corresponding to the volume-rate $F_s = F_{clk}/N_1N_2N_3$ Hz. For a light field having dimensions $N_1 \times N_2 \times N_3 \times N_4$, the architecture completes the filtering operation in $T_o = 2N_1N_2N_3N_4/F_{clk}$. For the example 2 shown in Table 1, the light field size

is $16 \times 16 \times 128 \times 128$. This design finishes the filtering operation in 0.24 s for a maximum operating frequency of 34.38 MHz.

5 Experimental verification

5.1 Host-embedded FPGA

In the following sections we describe a series of filter implementations for two design examples featuring differing light field geometries. We begin with verification on a host-embedded Xilinx Virtex-6 FPGA ML605 Evaluation Kit, for which the memory buffer of size $N_1 N_2 N_3$, depicted in Fig. 2, was implemented on the host PC.

Design Example 1 is a gantry-measured light field. The camera gantry, depicted in Fig. 7 (Dansereau 2003), translated a camera on a moving platform through 32×32 locations in the n_1, n_2 plane. Each image is of resolution 256×256, yielding a light field of $N_1 = N_2 = 32$ and $N_3 = N_4 = 256$. The test scene consists of a poster of a supernova image, in front of which a beer coaster is held in place by a wooden dowel. The poster and coaster are located at depths of 66 and 48 cm, respectively.

The final output of $H_2(\mathbf{z})$ for this example is shown in Fig. 8b and one of the 32×32 images of $w(\mathbf{n})$ is shown in Fig. 8a. Observe that the poster, at passband depth $d_p = 66$ cm, is enhanced, while the other scene elements are attenuated. The dark edges in the output are due to a non-zero passband delay, and can be corrected by using zero phase filtering (Dansereau 2003), in which the filtering operation is repeated with reversed directions of recursion.

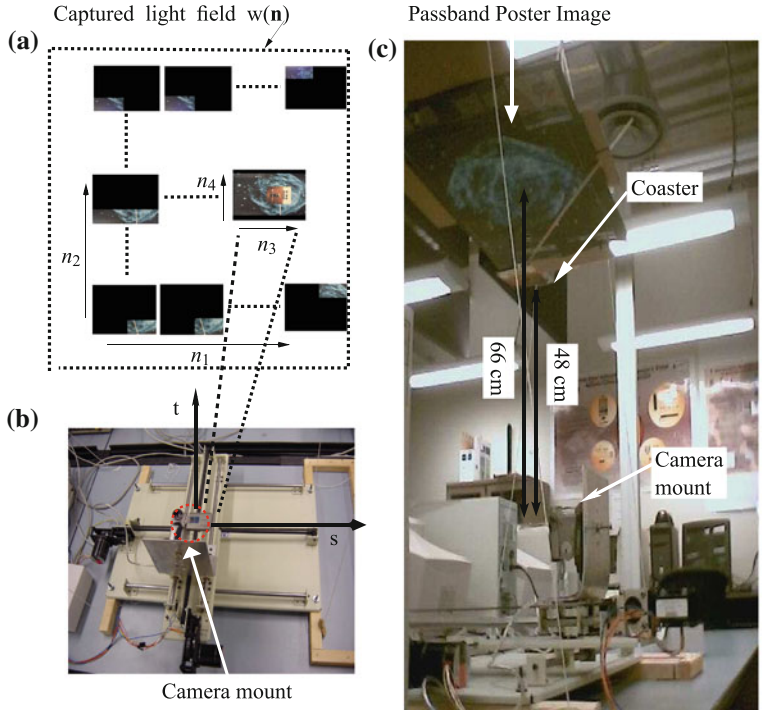

Fig. 7 **a** Captured light field $w(\mathbf{n})$, **b**, **c** Gantry apparatus used to capture the light field (Dansereau 2003)

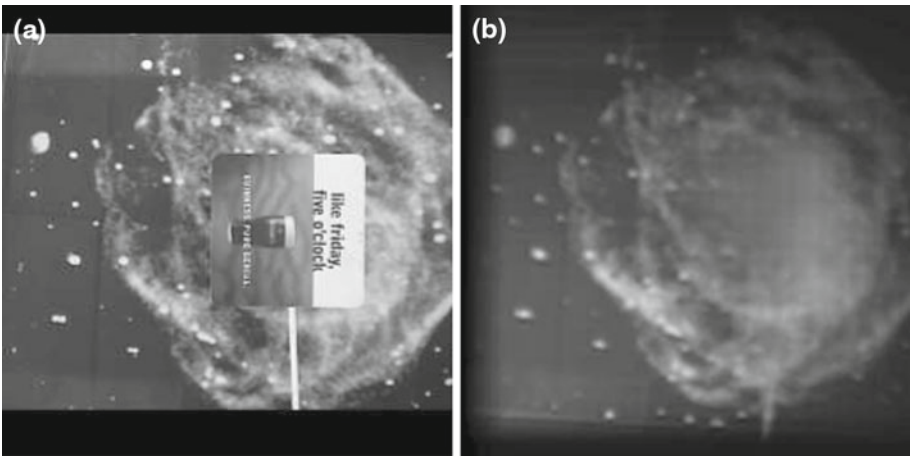

Fig. 8 **a** Original image with the coaster occlusion captured from the input light field (Dansereau 2003) **b** depth filtered output image captured from the output of $H_2(\mathbf{z})$ in the proposed hardware architecture

Design Example 2 was obtained from the Stanford Light Field Archive. Also captured using a gantry, this light field consists of a 16×16 array of images, each of which was downsampled to 128×128 samples. The test scene consists of toy Humvee and a toy soldier occluded by dense foliage. The passband in this example was selected so as to extract the toy Humvee while attenuating the dense foliage.

One of the 16×16 images of Example 2 is shown in Fig. 9a, the ideal depth-filtered output as generated using Matlab is shown in (b), and the hardware output is shown in (c). The Humvee has been successfully enhanced and the occluding dense foliage has been attenuated. The FPGA resource usage and maximum operating frequencies for the two design examples that were physically implemented in the Xilinx ML605 FPGA rapid prototyping system are summarised in Table 1.

5.2 Hardware simulation in BEE3

The FPGA realizations described above provide reconfigurable logic-based rapid prototyping for hardware-in-the-loop simulation, verification and validation of the register transfer language (RTL) code. This FPGA-based hardware emulation provides concrete evidence of the correctness of the digital design. Once thoroughly tested on-FPGA, the RTL can be synthesized in custom ASICs using Cadence design automation tools, as described in the next section. However, prior to constructing custom silicon it would be desirable to validate the full system on-FPGA, without assistance from externally-implemented memory buffers. To this end, we employ a Berkeley Emulation Engine (BEE3).

The BEE3 is a state of the art hardware emulation engine consisting of four Xilinx Virtex 5 FPGAs connected in a ring. With a development environment which runs on top of the Matlab Simulink framework, this system provides the necessary hardware interfaces and software drivers to allow rapid prototyping of complete complex digital designs with minimum overhead on low level configuration. The BEE3 has applications in wireless communication, aerospace and defense, high-speed networking, computer architecture and high definition video imaging (http://beecube.com/applications/; Davis et al. 2009; Yu et al. 2011; Muhlbach and Koch 2010).

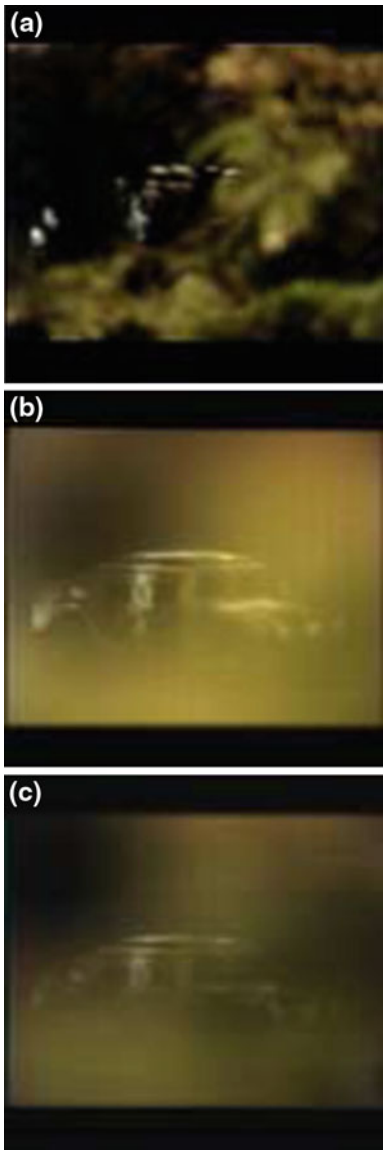

Fig. 9 **a** One of the example light field images, where the headlights and front part of the Humvee is covered by foliage in between the vehicle and the light field camera array, **b** ideal depth filtered Humvee image obtained from MATLAB, and **c** depth filtered Humvee obtained from the FPGA-based hardware implementation. The headlights and front part of the Humvee is clearly visible in both MATLAB implementation as well as the fixed-point realization on FPGA, which indicates that the 4-D IIR filter implementations are enabling the viewing of objects that are occluded using multi-dimensional IIR linear filtering

We achieved full hardware emulation of the two design examples in the BEE3, including memory buffers of size $N_1N_2N_3$, which we implemented in block RAM. High speed connectivity was achieved via 1 Gbps ethernet adapters, allowing large 4-D light field test vectors to be efficiently pushed through the FPGA realization. The resulting implementations allowed complete, robust verification of the RTL code prior to mapping to silicon. The implementations in examples 1 and 2 had maximum clock rates of 36.44 and 37.31 MHz, respectively, implying 4-D maximum light field frame rate of 0.27 Hz for Example 1 (light field size $32 \times 32 \times 256 \times 256$) and a maximum frame rate of 4.44 Hz for Example 2 (light field size $16 \times 16 \times 128 \times 128$). Example 1 was operated at a lower speed than the

Table 2 FPGA resources and parameters for example 1 and example 2 designs in the BEE3 system

FPGA	Example 1						Example 2	
	$H_1(z)$			$H_2(z)$			$H_1(z)$	$H_2(z)$
	A	B	C	A	B	C	A	A
Max frequency (MHz)	38.30	98.39	105.42	36.44	98.39	105.42	38.63	37.32
Number of slice LUTs	14,459	2,084	2,084	14,454	2,084	2,084	13,207	13,210
Number of slice registers	12,256	1,477	1,477	12,256	1,477	1,477	12,264	12,244
Number of occupied slices	7,241	7,64	7,79	7,179	7,64	7,79	6,975	6,787
Number of LUT flip flop pairs	20,125	2,352	2,397	20,131	2,352	2,352	18,970	18,831
Number of DSP48s	33	3	3	33	3	3	39	39

maximum because we used an external control signal for the block RAM, which was in turn mapped into two FPGAs. Therefore, the frame rate on the BEE3 is 0.017 Hz which is 16 times slower than the maximum frame rate which was obtained by FPGA realization. The maximum frame rate for example 2 remained to be 4.44 Hz because the whole system was implemented in a single FPGA. The resource consumptions as well as the corresponding maximum operating frequencies for the two design examples implemented in the BEE3 system is summarised in Table 2. Comparing Table 1 with Table 2, the amount of resources required for the BEE3 designs are much higher; this is due to the fact that the BEE3 design has an embedded processor and other peripheral controllers implemented inside the FPGA to support the ASIC prototyping and digital verification functionality.

5.3 ASIC synthesis using 45 nm CMOS

The two design examples were synthesized for ASIC using the Cadence Encounter RTL Compiler for 45 nm technology. Area, power, and speed results are presented in Table 3, for an ASIC implementation running at a typical operating supply voltage of 1.1 V and temperature of 27 Celsius. The light field frame rate achievable for Example 1, at a maximum operating frequency of 154.4 MHz, was 1.15 Hz; and for Example 2, at a maximum operating frequency of 153.3 MHz, was 18.286 Hz. These represent significant improvements in speed over the FPGA-based implementations. The fabrication of the ASIC synthesis has not been attempted due to prohibitive cost. However, for digital ASICs, FPGA-based RTL co-simulation in a hardware in the loop verification scheme coupled with ASIC synthesis results provide compelling evidence of performance even when the physically fabricated CMOS chips are not available.

Table 3 Speed of operation, power consumption and area utilization for an ASIC implementation of the 4-D integral form filter (45 nm technology)

Architecture	Area (mm^2)	Static power (mW)	Dyn. power (mW)	Total power (mW)	Max. freq. (MHz)
$H_1(z)$ *Example*1	2.836	23.180	4,151.403	4,174.584	157.6
$H_2(z)$ *Example*1	2.826	23.125	4,111.190	4,134.325	154.4
$H_1(z)$ *Example*2	1.734	13.371	2,400.358	2,413.729	153.3
$H_2(z)$ *Example*2	1.668	12.830	2,370.041	2,389.872	157.38

6 Conclusions

In this contribution, we proposed a digital VLSI architecture for the real-time implementation of 4-D IIR frequency-planar filters for light field based depth filtering applications. The proposed filter architecture employs a novel SFG based on discrete spatial integrators. Such integral-form SFGs exhibit improved sensitivity properties for perturbations in filter coefficients. We used first order sensitivity analysis of the 4-D filter transfer function to show that the proposed architecture yields a 92.9 % reduction in the maximum gain error in frequency response at a fractional precision of 12 bits, when compared with a direct-form architecture. We used two example light field geometries to verify the functionality of the hardware implementation. Verification was completed in three stages: first on a host-embedded FPGA, then on a standalone Berkeley Emulation Engine (BEE3), and finally on a 45 nm CMOS ASIC up to the synthesis level. Measured 4-D unit impulse responses from FPGA implementation were transformed to the 4-D frequency domain, and shown to conform closely to the desired 4-D frequency response obtained in closed-form. The filter outputs were also shown to display the desired depth selectivity by enhancing passband elements while attenuating undesired scene elements. The BEE3 implementations operate at 36.44 and 37.31 MHz, respectively for the two light field examples, while ASIC synthesis in 45 nm CMOS verify an operating frequency around 150 MHz.

Reducing the computational complexity using 4-D fast algorithms, minimizing critical path delay, reducing quantization effects and estimating and optimizing for power consumption remain as future work.

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